

RELIABILITY SCOPE

INTRODUCTION

In order to achieve a high competitive Quality and Reliability level of its products, EM has developed a comprehensive Reliability Control System. This system finds its fundamentals in the ISO 9001:2000 and ISO/TS 16949:2002. EM's Reliability Control System is composed of four main blocks:

- Reliability in Design and Development
- Reliability through Qualification
- Process Control
- Reliability Monitoring of products

This report outlines the Reliability Control System and details the Reliability Monitoring System of Products (RMP) as well as presenting data on the results of this system.

RELIABILITY CONTROL SYSTEM

Adequate design-proving activities are established for each new design and include:

Simulation, Design & Electrical Rule Checking, Design Acceptance (including viability in user application) and Device Qualification (including reliability assessment).

Reliability through Qualification

This system is used to ensure that released products are designed, processed, packaged and tested to meet both design performances and strict reliability objectives. It is using the same tests described in the Reliability Monitoring System of products. In addition and depending on product type, some additional tests are performed:

- PC Preconditioning for SMD products
- EV External visual
- LI Lead Integrity
- BPS Bond Pull Strength
- BS Bond Shear
- ESD Electrostatic Discharge
- LU Latch-up
- SD Solderability
- GL Electro-Thermally Induced Gate Leakage
- ED Electrical Distribution

Process Control

Process quality control consists of routine monitoring of important process parameters such as resistivities, oxide thickness, mask alignment, dimensional checks, defect densities, bump parameters, bond strength and shear test measurements.

Reliability Monitoring System

EM monitors on a continuing basis the reliability of devices representative of those shipped from production. The program is based on monitoring key products within each generic Technology and package family.

The results from the RMS are reported yearly. Intermediate results are also available upon request.

Reliability Monitoring is performed by using various products in each generic Technology and package family. The products used to sample these processes include diverse:

- Diffusion lots
- Die sizes
- Percentage of analog – digital blocks
- With / without EEPROM blocks
- Package assembly lots
- Package pin count
- Package types
- Preferred Assembly sites

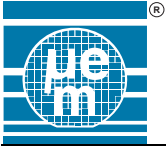
Products are selected from the standard manufacturing flow and spread over production time. Typically, 32 samples are used for one reliability test. A reference sample of the same lot is kept outside of the reliability test and used to validate the test setup before each measurement step. No preliminary Burn-In is performed on devices prior to reliability testing. There fore, result data contain early life failures.

Performed tests are:

- HTOL High Temperature Operating Life
- HTB High Temperature Bake
- THB Temperature Humidity Bias
- AC Autoclave
- TC Temperature Cycling
- ET EEPROM Data Endurance / Retention

Technology families are:

- HCMOS 3µm
- ALP2 2µm
- ALP1 1µm
- ALP05 0.5µm



FAILURE RATE CALCULATION

In determining device failure rates, it is important to fully understand the failure rate characteristics as a function of time. EM determines such characteristics by performing accelerated stress tests at high temperature and maximum voltage. EM failure rate calculations are based on high temperature accelerated results where the thermal activation energy E_a , is equated to 0.8 eV. The number of total device hours realized at the accelerated temperature is then accurately extrapolated to an ambient temperature of 55°C by means of the Arrhenius equation:

$$t_1 = t_2 \cdot e^{\frac{E_a}{K} \left(\frac{1}{T_1} - \frac{1}{T_2} \right)}$$

Where:

t_1, t_2 = MTBF at temperatures T_1 and T_2 respectively

T_1, T_2 = temperature in °K

K = Boltzmann's Constant (8.62 E-5 eV/ °K)

E_a = Thermal Activation Energy in eV

The reciprocal ratio of MTBF in terms in t_1 and t_2 provides the acceleration factor between the temperatures T_1 and T_2 .

The failure rate can be calculated at any confidence level by applying the relationship:

$$\text{Failure Rate} = \frac{\chi^2(CL, 2r + 2)}{2nt}$$

Where:

χ = Chi square function

CL = Confidence level expressed as a decimal

r = number of rejected parts

n = number of parts tested

t = total test time

The failure rate can be expressed in terms of ppm per 1000 hours, or number of failures in 10E9 device hours. This result will be expressed in FITs. 100 Fits equal 0.01% fail per 1000 device hours.

RELIABILITY TEST DESCRIPTION

Devices submitted to Reliability test are fully measured before and after Reliability testing, using the production test equipment. Intermediate measurement steps are made if specified in the detailed test plan.

HTOL High Temperature Operating Life

The operating life-test is performed for the purpose of demonstrating the quality and reliability of devices subjected to the specified conditions over an extended time period. Either a static or a dynamic condition may be used, depending on the circuit type. The devices are supplied at the maximum rated voltage of the data sheet. Unless otherwise specified in the detailed test plan, the test is run at a temperature of 150°C for 1000 hours. The extrapolation of data for Fit rate does not include electrical acceleration. (Max. rated voltage versus operating voltage). First figures are calculated for a confidence level of 60% & 95%. Fits for a confidence level of 60% & 95% show the strong influence of the number of tested samples for the statistical prediction of the Fit rate.

HTB High Temperature Bake

The High Temperature Storage Bake is used for the purpose of determining the effect of storing packaged devices at elevated temperature, without electrical stress applied. Unless otherwise specified in the detailed test plan, the test is run at an ambient temperature of 150°C for 1000 hours.

THB Temperature Humidity Bias

The Temperature Humidity Bias test is performed for the purpose of evaluating the resistance of non-hermetic packaged devices operating in humid environment. Either a static or a dynamic condition may be used, depending on the circuit type. The devices are supplied at the maximum rated voltage of the data sheet. Unless otherwise specified in the detailed test plan, the test is run at 85°C / 85% relative humidity for 1000 hours.

AC Autoclave

The Autoclave test is performed for the purpose of evaluating the humidity penetration resistance of non-hermetic packaged devices. The circuits are not biased during the test. Unless otherwise specified in the detailed test plan, the test is run at 15psi / 121°C for 96 hours. (Saturated).

TC Temperature Cycling

The Temperature Cycling test is performed for the purpose of determining the resistance of devices to alternate exposures at extreme temperatures. Package strength, bond quality and consistency of assembly process are stressed using this environment. The circuits are not biased during the test. Unless otherwise specified in the detailed test plan, the test is run at -50°C / 10min. ; +150°C / 10 min. for 1000 cycles.

ET E²PROM Data Endurance / Retention

Data Endurance test is performed for the purpose of determining the resistance of a device to successive Erase / Write cycles of the E²PROM. One cycle is defined as one erase and one write procedure of the whole E²PROM. The write procedure writes the E²PROM to 1. Unless otherwise specified in the detailed test plan. The test is run up to 100'000 cycles, at room temperature.

Data retention test is performed for the purpose of determining the resistance of an E²PROM to charge loss of the memory cells. This test is conducted after a Data Endurance test. Unless otherwise specified in the detailed test plan, the test is run at an ambient temperature of 150°C for 1000 hours. (Same procedure as HTB).

RELIABILITY DATA SUMMARY

Other generic reliability data are available upon request. Please contact our Customer Service.